AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph on page 8 starting at line 13 as follows:

Figure 5 is a flowchart of a method 500 for fabricating a memory device in accordance with embodiments of the present invention. In step 510 of Figure 5, a dopant is deposited in a first region of a semiconductor substrate of a memory device. Referring now to Figure 6A, dopants are deposited in impurity concentrations 612 and 613 of first region 610 of a memory device 600. In embodiments of the present invention, previous fabrication steps have been preformed upon memory device 600 such as deposition of n-type wells (not shown), deposition of a high voltage p-type well 650 in the core region, and fabrication of a gate array 611 upon semiconductor substrate 605. Additionally, the gate array 621 of a memory cell has been fabricated upon semiconductor substrate 605 in a second region 620. In embodiments of the present invention, first region 610 corresponds to a periphery region of memory device 600 and second region 620 corresponds to the core array region. In the embodiment of Figure 6A, the gate length of ~~date~~ gate array 611 is longer than the gate length of gate array 621.

Please amend the paragraph on page 9 beginning at line 4 as follows:

In step 520 of Figure 5, an annealing process is performed upon the semiconductor substrate. Referring now to Figure 6B, when the annealing process is performed, the dopants deposited in impurity concentrations 612 and 613 are diffused into the surrounding substrate 605. Annealing is a process used in the manufacture of semiconductor devices in which the device is subjected to a high heat for a controlled amount of time. Annealing is used to repair damage to semiconductor substrate 605 as a result of implanting the dopants in step ~~610~~ 510. Annealing is also used to activate the dopants and to restore some electron mobility that is lost during step ~~610~~ 510. Annealing characteristics depend, among other things, upon the type and dose of dopant used in step ~~610~~ 510. Therefore, the type and dose of dopant used in step ~~610~~ 510, as well as the desired electrical characteristics (e.g. junction depth, channel length, and electrical resistance, etc.) of the finished peripheral device are taken into account when selecting the parameters of the annealing in step ~~620~~ 520. In one embodiment, a rapid thermal annealing (RTA) process is used in step 520 of the present

invention. However, while the present embodiment recites RTA specifically, the present invention is well suited to utilize other processes as well.

Please amend the paragraph on page 9 beginning at line 18 as follows:

In embodiments of the present invention, the parameters of the annealing process of step 520 are selected to only partially diffuse the dopants. In other words, the parameters of the annealing process are chosen such that the dopants are not diffused to the final or optimal desired level of diffusion. Thus, if the final desired level of diffusion is considered 100% diffused, the parameters of the annealing process in step 520 are some partial value such as, for example, a 20% diffusion, a 25% diffusion, etc. Again, while the present embodiment recites these specific values, the present invention is well suited to a variety of values for step 520. Referring again to Figure 6B, following the annealing process of step ~~620~~ 520, the dopants in impurity concentrations 612 and 613 are diffused to create impurity concentrations 614 and 615 respectively. That is the dopants in impurity concentration 612 are diffused into substrate 605 to create impurity concentration 614, and the dopants in impurity concentration 613 are diffused into substrate 605 to create impurity concentration 615.

Please amend the paragraph beginning on page 9 at line 30 as follows:

In step 530 of Figure 5, a depositing of a dopant in a second region of the semiconductor substrate is performed. Referring now to Figure 6C, impurity concentrations 622 and 623 are deposited in second region 620 of semiconductor substrate 605. In the embodiment of Figure 6C, second region 620 comprises the core array of a memory device such as a flash memory device. As described in the above discussion of step 510, there are a variety of methods for depositing impurity concentrations 622 and 623 in embodiments of the present invention. Impurity concentrations 622 and 623 may be, for example, the source and drain regions of a memory cell in the core array of memory device 600.

Please amend the paragraph beginning on page 10 at line 18 as follows:

In the embodiment of Figure 6D, the second annealing process of step 540 comprises a full annealing of the dopants in impurity concentrations 622 and 623.

In other words, the parameters of the annealing process of step 540 are selected to create impurity concentrations 624 and 625 and are based upon the electrical characteristics of the memory cell in core area 620. Additionally, the second annealing process of step 540, in conjunction with the annealing process of step 520, comprise a cumulative annealing process for the dopants deposited in first region 610 (e.g. impurity concentrations 612 and 613). In other words, having prior knowledge of the process parameters of the annealing process of step 540, the process parameters of the annealing process of step 520 are selected such that the cumulative result of both annealing processes result in impurity concentrations 616 and 617. For example, if the parameters of the second annealing process of step 540 comprise a 25% diffusion of total desired diffusion of the dopants in the impurity concentrations in first region 610, the parameters of the first annealing process are selected to comprise a 75% diffusion of the dopants in region 610. Thus, the cumulative effect of both of the annealing processes results in a 100% diffusion of the dopants in first region 610 and in second region 620. It is appreciated that the process parameters of the cumulative annealing process of the dopants in first region 610 are selected based upon the electrical characteristics of the semiconductor device in first region 610. Referring now to Figure 6E, as a result of the cumulative annealing process of the present invention, a semiconductor device in first region 610 is fabricated upon a semiconductor substrate that is of a greater scale than a second semiconductor device in second region 620 of the same semiconductor substrate.

Please amend the paragraph beginning on page 13 at line 12 as follows:

In step 820 of Figure 8, a dopant is deposited in a second region of the semiconductor substrate. Referring again to Figure 6C, impurity concentrations 622 and 623 are created by depositing a dopant in second region 620 of Figure 6C.